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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/073,999	02/14/2002	Ken Takeuchi	001701.00140	9741

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EXAMINER	
HO, HOAI V	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 07/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/073,999	TAKEUCHI ET AL.	
	Examiner	Art Unit	
	Hoai V. Ho	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *47-60,62,63,65 and 66* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *48-50, 52-54, 56-58, 62, 63, 65 and 66* is/are allowed.

6)☒ Claim(s) *47,51,55,59 and 60* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/667,610.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/7/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment

1. This office action is responsive to communication(s) filed on June 14, 2006.

2. Claims 47-60, 62, 63, 65 and 66 are presented.

Claim Objections

3. Claims 48 and 49 are objected to because of the following informalities:

Claim 48, line 13, change "said" in a first occurrence of a phrase "while said program voltage is supplied to said second memory cell" to --a--.

Claim 49, line 3, change "a" in a first occurrence of a phrase "while a program voltage is supplied to said second memory cell" to --said--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an

international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims 47, 51, 55, 59 and 60 are rejected under 35 U.S.C. 102(e) as being anticipated by Tanaka USP 6125052.

As per claim 47, Fig. 5 of Tanaka is directed to a nonvolatile semiconductor memory comprising a first string line (BLi) including a first memory cell (M) and a first select transistor (S) connected in series; a second string line (BLi+1) including a second memory cell (M) and a second select transistor (S) connected in series; a first bit line (BLi) connected to said first string line; a second bit line (BLi+1) connected to said second string line being different from said first bit line; a common node (a common line connects to Qn10 and Qn21) connected to one ends of said first and second bit lines; and a common latch (10) connected to said common node, wherein first program/read data of said first memory cell is latched in said common latch circuit, while second program/read data of said second memory cell is held by said second bit line (col. 5, lines 41-43, col. 7, lines 7-22, 47-67 and col. 17, lines 21-22).

As per claim 51, Fig. 5 of Tanaka is directed to wherein said first memory cell (M connects to WL1) and said second memory cell (M connects to WL2) are connected to different word lines (WL1 and WL2).

As per claim 55, Fig. 5 of Tanaka is directed to a nonvolatile semiconductor memory comprising a first string line (BLi) including a first memory cell (M) and a first select transistor (S) connected in series; a first bit line (BLi) connected to said first string line; a second bit line (BLi+1) being different from said first bit line; a common latch circuit (10) having a common

node (a common line connects to Qn10 and Qn21) connected to one ends of said first and second bit lines latching program/read data; and said common latch circuit (10) connected to said common node, wherein first program/read data of said first memory cell is held by said second bit line (col. 7, lines 56-61, col. 17, lines 21 and 22).

As per claims 59 and 60, Tanaka discloses wherein said program/read data is held by said first or second bit line, a potential of a bit line adjacent to said first or second bit line is at a fixed potential (col. 10, lines 32-34).

6. Claims 47, 51, 55, 59 and 60 are rejected under 35 U.S.C. 102(e) as being anticipated by Shibata et al. USP 6122193 (IDS).

As per claim 47, Figs. 8 and 9 of Shibata are directed to a nonvolatile semiconductor memory comprising a first string line (BLi) including a first memory cell (M) and a first select transistor (SGD) connected in series; a second string line (BLi+1) including a second memory cell (M) and a second select transistor (SGD) connected in series; a first bit line (BLi) connected to said first string line; a second bit line (BLi+1) connected to said second string line being different from said first bit line; a common node (a common line connects to BLC1 and BLC2) connected to one ends of said first and second bit lines; and a common latch (10-i) connected to said common node, wherein first program/read data of said first memory cell is latched in said common latch circuit, while second program/read data of said second memory cell is held by said second bit line (abstract, col. 6, lines 51-57 and col. 7, lines 12-14).

As per claim 51, Fig. 5 of Shibata is directed to wherein said first memory cell (M connects to WL1) and said second memory cell (M connects to WL2) are connected to different word lines (WL1 and WL2).

As per claim 55, Fig. 5 of Shibata is directed to a nonvolatile semiconductor memory comprising a first string line (BLi) including a first memory cell (M) and a first select transistor (SDG) connected in series; a first bit line (BLi) connected to said first string line; a second bit line (BLi+1) being different from said first bit line; a common latch circuit (10-i) having a common node (a common line connects to BLC1 and BLC2) connected to one ends of said first and second bit lines latching program/read data; and said common latch circuit (10-i) connected to said common node, wherein first program/read data of said first memory cell is held by said second bit line (abstract, col. 3, lines 45-46, col. 7, lines 15-18, col. 25, lines 29-35 and col. 26, lines 31-34).

As per claims 59 and 60, Shibata discloses wherein said program/read data is held by said first or second bit line, a potential of a bit line adjacent to said first or second bit line is at a fixed potential (col. 13, lines 44-49).

7. Claims 47, 51 and 55 are rejected under 35 U.S.C. 102(e) as being anticipated by Nobukata USP 6058042.

As per claim 47, Fig. 2 or 5 of Nobukata is directed to a nonvolatile semiconductor memory comprising a first string line (BL1) including a first memory cell (MT0A) and a first select transistor (SG1A) connected in series; a second string line (BL2) including a second memory cell (MT1B) and a second select transistor (SG1B) connected in series; a first bit line (BL1) connected to said first string line; a second bit line (BL2) connected to said second string line being different from said first bit line; a common node (a common line connects to NT3 and NT4, or SA21) connected to one ends of said first and second bit lines; and a common latch (2 or 12) connected to said common node, wherein first program/read data of said first memory cell is

latched in said common latch circuit, while second program/read data of said second memory cell is held by said second bit line (col. 2, lines 7-10 and col. 15, lines 21-29).

As per claim 51, Fig. 2 or 5 of Nobukata is directed to wherein said first memory cell (MT0A) and said second memory cell (MT1B) are connected to different word lines (WL0 and WL1, respectively).

As per claims 55, Fig. 2 or 5 of Nobukata is directed to a nonvolatile semiconductor memory comprising a first string line (BL1) including a first memory cell (MT0A) and a first select transistor (SG1A) connected in series; a first bit line (BL1) connected to said first string line; a second bit line (BL2) being different from said first bit line; a common latch circuit (2 or 5) having a common node (a line connects to NT3 and NT4, or SA21) connected to one ends of said first and second bit lines latching program/read data; and said common latch circuit connected to said common node, wherein first program/read data of said first memory cell is held by said second bit line (col. 5, lines 38-57).

8. The prior art made of record and not relied upon is considered pertinent to applicants= disclosure. Park et al. (USP 5966326) and Lee (USP 5748529) disclose a non-volatile memory device with page buffers.

Allowable Subject matter

9. Claims 48-50, 52-54, 56-58, 62, 63, 65 and 66 are allowed.

10. The following is a statement of reasons for the indication of allowable subject matter:

Claims include allowable subject matter since the prior art made of record and considered pertinent to the applicants' disclosure, taken individually or in combination, does not teach or suggest the claimed invention having while said program voltage is supplied to said second

memory cell, a verify read operation to verify whether said first memory cell has been programmed sufficiently, is carried out by said common latch circuit, and while said program voltage is supplied to said first memory cell, the program of data said second memory cell held by said second bit line is latched in said common latch circuit and a verify read operation to verify whether said second memory cell has been programmed sufficiently, is carried out by said common latch circuit in claims 48 and 50; after said program voltage is supplied to said first memory cell, said common latch circuit is electrically connected to said second bit line and the program data of said first memory cell held by said second bit line is latched in said common latch circuit; and a verify read operation to verify whether said first memory cell has been sufficiently programmed, is carried out using said program data latched in said common latch circuit in claim 56; and program data of said second memory cell is held by at least one of said third and fourth bit lines while a program voltage is supplied to said first and second memory cells; a verify read operation to verify whether said first memory cell has been sufficiently programmed, is carried out by said common latch circuit, and program data of said second memory cell is held by said fourth bit line while conducting the verify read operation of said first memory cell; and said common latch circuit and said fourth bit line are electrically connected to each other, after the program data of said second memory cell held by said fourth bit line is latched in said common latch circuit, a verify read operation to verify whether said second memory cell has been sufficiently programmed, is carried out using the program data of said second memory cell held by said common latch circuit, and while conducting a verify read operation of said second memory cell, the program data of said first memory cell is held by said second bit line in claim 57; and a combination of other limitations thereof as recited in claims.

11. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

12. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02 (b)).

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoai V. Ho whose telephone number is (571) 272-1777. The examiner can normally be reached 7:00 AM -- 5:30 PM from Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is (571)-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

hvh
June 28, 2006

Hoai V. Ho
Primary Examiner
Art Unit 2818